Distributed Parallel Operation of Modified Deadbeat Controlled UPS Inverters

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***Abstract-* A novel control scheme is proposed for the parallel operation of UPS modules. In this scheme, each UPS in parallel is controlled by a modified deadbeat control method. The traditional deadbeat control has a robust problem to parameter imprecision, which restricts its application. A proportional element is added in the proposed method to solve this problem. The modified deadbeat controlled inverter has good static performance and fast dynamic response and is insensitive to parametric deviation. A distributed control method is used here to realize parallel operation. All the UPS modules are connected by two common lines. One provides a phase signal to synchronize the output voltage. The other one provides the average current signal for the instantaneous average current-sharing control. Experiments are carried out on three 1kVA on-line UPS modules. The theoretic analysis and experimental results show that the system acts satisfactorily both in steady state and dynamic process. The load distribution among UPS modules is precise in different load conditions, and the real abundance can be achieved.**

I. INTRODUCTION

Nowadays, uninterrupted power supplies are widely used to provide continuous electrical power to loads that cannot afford unexpected power failure. Furthermore, the parallel operation of modularized UPS units can be a solution to both capability and reliability. It is convenient and economic to change the power capacity by adjusting the number of UPS units in parallel. Besides, *N*+*X* redundancy operation can greatly improve the reliability of the system. Recently, many scholars focus on the research of the parallel operation and the digital control schemes of UPS inverters. To achieve the good performance of a parallel UPS system, there are two main requirements: (1) High performance of each UPS in parallel. The dynamic response should be fast, and the output voltage should have a low THD. (2) Proper current distribution among inverters. For this target, the output voltage of each UPS should have the same amplitude, frequency, and phase. A current-sharing control is also necessary to reduce the circular current.

To limit the output voltage distortion and improve the performance of UPS inverters, various digital control methods have been proposed, such as repetitive control, deadbeat control, sliding mode control, and etc. Derived from state equations, deadbeat control has fast dynamic response and can eliminate the state variable errors in several control periods. However, the high sensitivity to parameter mismatches, model uncertainties, and noise on the sensed variables of the deadbeat control still restricts its application [1,2,3]. This problem can be much more serious in the parallel operation of several deadbeat controlled UPS modules.

For a parallel system, each output voltage of the UPS modules should have the same amplitude, frequency and phase; otherwise the circular current would increase power loss and even make the system unstable. Besides, a current-sharing control is indispensable to ensure the proper current distribution among modules even if there is some difference between the outputs of UPS modules. Among all the current-sharing control schemes, the instantaneous current-sharing schemes have good performance both on current distribution and voltage regulation [4,5,6]. They can be classified as master-slave current-sharing scheme, average current-sharing scheme, maximum current-sharing scheme, and circular-chain current-sharing scheme. Their common advantage is that the current is regulated at every switch period so that the system has fast dynamic response when load changes.

In this paper, the distributed parallel operation of deadbeat controlled UPS inverters is realized in experiment based on DSP TMS320LF2407A. A modified deadbeat control scheme is proposed here. It can effectively improve the robustness of deadbeat control with the expense of a little increased static error and slower dynamic response. A novel distributed operation of UPS inverters with instantaneous average current-sharing scheme is implemented with two common lines providing synchronous phase signal and average current signal respectively.

II. MODIFIED DEADBEAT CONTROL

A. Systematic Analysis

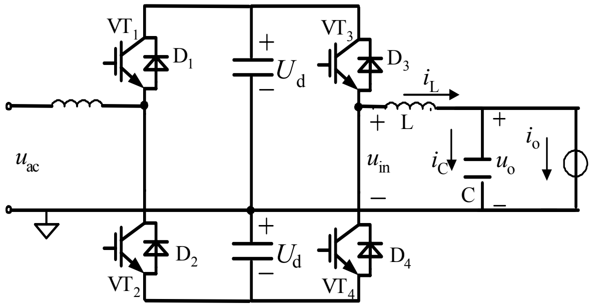


Figure 1. Diagram of a single-phase UPS

The circuit of a single-phase UPS is shown in Fig.1. It mainly consists of the rectifier part and the inverter part. Here we mainly focus on the inverter part. It usually has the inverter bridge, the output filter and the load. To simplify the analysis, the two capacitors in the DC side are supposed to have the same constant voltage U_d. u_{in} is the output voltage of inverter bridge, and in the two level pattern it is either $+U_d$ or $-U_d$.

If the output voltage u_o and the inductance current i_L are chosen as state variables, and the load current i_o is treated as disturbance, the system state equation is

$$\dot{\boldsymbol{x}} = \boldsymbol{A} \cdot \boldsymbol{x} + \boldsymbol{B} \cdot u_{in} + \boldsymbol{D} \cdot i_o \tag{1}$$

$$y = \boldsymbol{C}^T \cdot \boldsymbol{x} \tag{2}$$

where $\boldsymbol{x}=[u_o \quad i_L]^T$, $\boldsymbol{A}=[0 \quad 1/C \ ; \ -1/L \quad 0]$, $\boldsymbol{B}=[0 \quad 1/L]^T$, $\boldsymbol{D}=[-1/C \quad 0]^T$, $\boldsymbol{C}=[1 \quad 0]^T$.

The discrete state equation can be expressed as

$$x(k+1) = \boldsymbol{\Phi} x(k) + \mathbf{G}\Delta T(k) + \mathbf{P} i_o(k) + \mathbf{H} \tag{3}$$

where

$$\boldsymbol{\Phi} = e^{AT} = \begin{bmatrix} \psi_{11} & \psi_{12} \\ \psi_{21} & \psi_{22} \end{bmatrix} \tag{4}$$

$$\mathbf{G} = 2U_d e^{(AT/2)} \boldsymbol{B} = [g_1 \quad g_2]^T \tag{5}$$

$$\mathbf{P} = -\boldsymbol{A}^{-1}(I - e^{AT})\boldsymbol{D} = [p_1 \quad p_2]^T \tag{6}$$

$$\mathbf{H} = U_d \boldsymbol{A}^{-1}(I - e^{AT})\boldsymbol{B} = [h_1 \quad h_2]^T \tag{7}$$

T is the control period, $\Delta T(k)$ is the acting time of positive voltage $+U_d$ in the kth control period.

B. Traditional Deadbeat Method

The required pulse width $\Delta T(k)$ can be computed by making $u_o(k+1)$ in the first equation in (1) equal to the voltage reference $u_{ref}(k+1)$. The deadbeat control law is

$$\Delta T(k) = \frac{1}{g_1} u_{ref}(k+1) - \frac{\psi_{11}}{g_1} u_o(k) - \frac{\psi_{12}}{g_1} i_L(k) - \frac{p_1}{g_1} i_o(k) - \frac{h_1}{g_1} \tag{8}$$

Deadbeat control depends on the precise mathematical models of the controlled object. In ideal conditions, the calculating parameters used in (8) are identical with the actual parameters of the inverter. However, the precise systemic model is difficult to obtain, and the actual parameters may change during operation. Here we use symbols with '^'as calculating values and symbols without '^' as actual values. The actual control law of traditional deadbeat control can be rewrote as

$$\Delta T(k) = \frac{1}{\hat{g}_1} u_{ref}(k+1) - \frac{\hat{\psi}_{11}}{\hat{g}_1} u_o(k) - \frac{\hat{\psi}_{12}}{\hat{g}_1} i_L(k) - \frac{\hat{p}_1}{\hat{g}_1} i_o(k) - \frac{\hat{h}_1}{\hat{g}_1} \tag{9}$$

Fig.2 shows the discrete system block diagram of the traditional deadbeat control. The transfer function from $U_{ref}(z)$ to $\boldsymbol{X}(z)$ is

$$\frac{\boldsymbol{X}(z)}{U_{ref}(z)} = z[\mathrm{C}^T \hat{\mathrm{G}}(z\boldsymbol{I} - \boldsymbol{\Phi}) + \mathbf{G}\,\mathrm{C}^T \hat{\boldsymbol{\Phi}}]^{-1}\mathbf{G} \tag{10}$$

The transfer function from voltage reference to output voltage is

$$\begin{aligned} G_i(z) &= \frac{U_o(z)}{U_{ref}(z)} = \frac{\mathrm{C}^T \boldsymbol{X}(z)}{U_{ref}(z)} = z\,\mathrm{C}^T[\mathrm{C}^T \hat{\mathrm{G}}(z\boldsymbol{I} - \boldsymbol{\Phi}) + \mathbf{G}\,\mathrm{C}^T \hat{\boldsymbol{\Phi}}]^{-1}\mathbf{G} \\ &= [g_1 z^2 + (g_2\psi_{12} - g_1\psi_{22})z]/q(z) \end{aligned} \tag{11}$$

where

$$\begin{aligned} q(z) = {} & \hat{g}_1 z^2 + [g_1\hat{\psi}_{11} + g_2\hat{\psi}_{12} - \hat{g}_1\psi_{22} - \hat{g}_1\psi_{11}]z + g_2(\hat{\psi}_{11}\psi_{12} - \psi_{11}\hat{\psi}_{12}) \\ & + \psi_{21}(g_1\hat{\psi}_{12} - \hat{g}_1\psi_{12}) + \psi_{22}(\hat{g}_1\psi_{11} - g_1\hat{\psi}_{11}) \end{aligned}$$

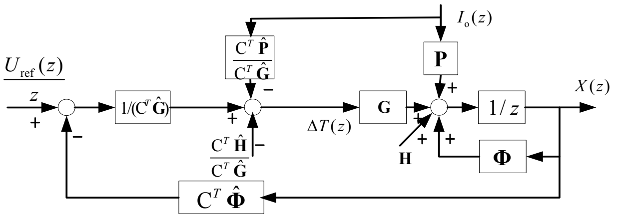
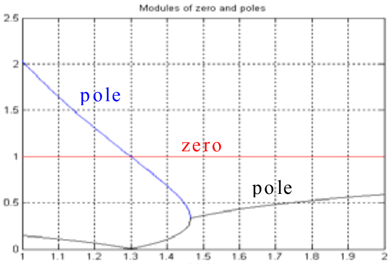


Fig.2 Discrete system block diagram of traditional deadbeat control

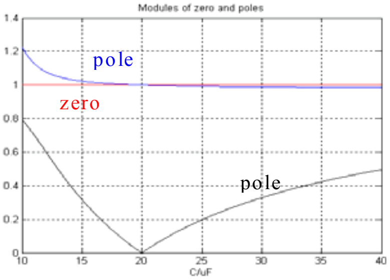
If the calculating values and the actual values are the same, its transfer function can be simplified as

$$G(z) = 1 \tag{12}$$

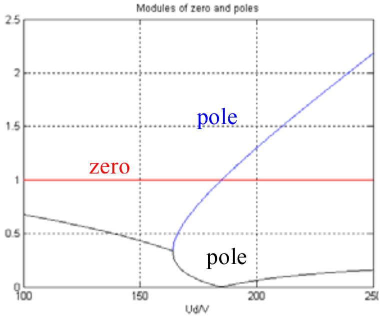
Equation (12) means that with the traditional deadbeat control, the output voltage follows the reference in case that there is no parametric mismatch. However, it is not always the case in practice. A typical UPS inverter is considered to study the influence of parametric deviation. The calculating parameters are: $\hat{U}_d$=185 V, $\hat{L}$=1.3 mH, $\hat{C}$=20 μ F. Fig.3(a) shows the module tracks of zero and poles of the transfer function in traditional deadbeat control, when L changes, and U_d and C are the same as calculating values. One zero of (11) always stays in origin and is not plotted. Similarly, Fig.3(b) and Fig.3(c) show the module tracks when C and U_d change respectively. According to the classical control theory, the modules of each pole should be less then 1 to ensure the system stable. When actual parameters match calculating values, the zeros counteract the poles, and we get (12). However, when there is parametric mismatch, the system can easily become unstable. As shown in Fig.3, when the actual inductance L is smaller than calculating inductance $\hat{L}$, or the actual capacitor C is smaller than $\hat{C}$, or the actual DC link voltage U_d is bigger than $\hat{U}_d$, the system has a pole outside the unit circle in Z-plane and becomes unstable. The poor robustness makes the traditional deadbeat control almost impracticable in UPS application.



(a) when L changes



(b) when C changes



(c) when U_d changes
Fig.3 Modules of zero and poles in traditional deadbeat control

C. Modified Deadbeat Method

To deal with the robust problem with deadbeat control and make it applicable in UPS, a modified control method is proposed here. As show in Fig.4, a proportional element k_w is added to the control diagram of the new method. Comparing Fig.2 and Fig.4, we can see that it returns to the traditional deadbeat control when k_w =1.

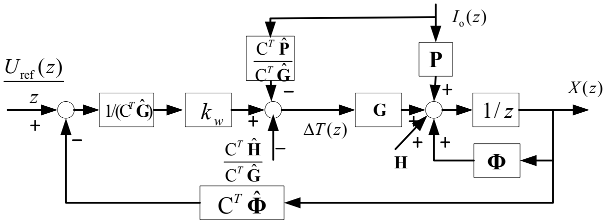


Fig.4 Discrete system block diagram of modified deadbeat control

The control law of the modified deadbeat method is

$$\Delta T(k)=\frac{k_w}{\hat{g}_1}u_{ref}(k+1)-\frac{k_w\hat{\psi}_{11}}{\hat{g}_1}u_o(k)-\frac{k_w\hat{\psi}_{12}}{\hat{g}_1}i_L(k)-\frac{\hat{p}_1}{\hat{g}_1}i_o(k)-\frac{\hat{h}_1}{\hat{g}_1} \qquad (13)$$

where usually $0<k_w<1$.

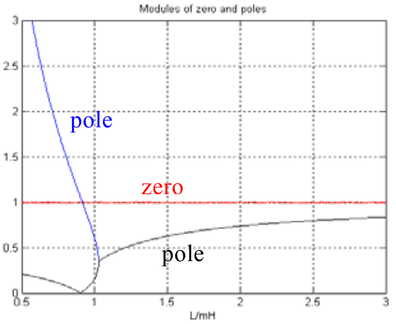
The transfer function from voltage reference to output voltage in the modified method is

$$G_i(z)=\frac{U_o(z)}{U_{ref}(z)}=\frac{C^T\boldsymbol{X}(z)}{U_{ref}(z)}=z\,C^T[\frac{C^T\hat{G}}{k_w}(z\boldsymbol{I}-\boldsymbol{\Phi})+\mathbf{G}\,C^T\hat{\boldsymbol{\Phi}}]^{-1}\mathbf{G}$$
$$=k_w[g_1z^2+(g_2\psi_{12}-g_1\psi_{22})z]/l(z) \qquad (14)$$

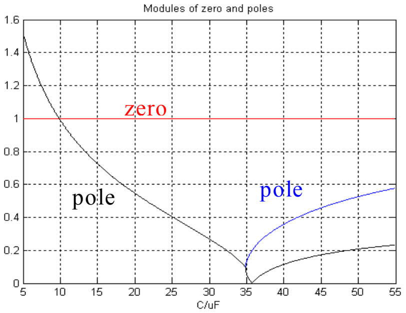
where

$$l(z)=\hat{g}_1z^2+[g_1\hat{\psi}_{11}k_w+g_2\hat{\psi}_{12}k_w-\hat{g}_1\psi_{22}-\hat{g}_1\psi_{11}]z+g_2k_w(\hat{\psi}_{11}\psi_{12}-\psi_{11}\hat{\psi}_{12})+\psi_{21}(g_1\hat{\psi}_{12}k_w-\hat{g}_1\psi_{12})+\psi_{22}(\hat{g}_1\psi_{11}-g_1\hat{\psi}_{11}k_w)$$

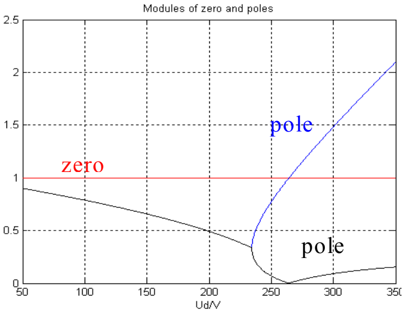
The proposed deadbeat control with a proportional element has better robustness compared with the traditional method. Fig.5 shows the module tracks of zero and poles of the transfer function in the modified deadbeat control (k_w =0.7) when the actual inductance L, the actual capacitor C, and the actual DC link voltage U_d change respectively. We can see that in this case the system can remain stable as long as L is larger than 0.913mH (70.23% $\hat{L}$), C is larger than 9.82 μ F (49.1% $\hat{C}$), and U_d is smaller than 264.5V (146.94% $\hat{U}_d$). Compared with the situation in traditional deadbeat control method, it is obvious that constraints in the proposed method are much less strict, and the control method has better robustness when actual parameters deviate from calculating parameters.



(a) when L changes



(b) when C changes



(c) when U_d changes
Fig.5 Modules of zero and poles in modified deadbeat control

The proportional element improves the robustness of the deadbeat control, while it causes a little increased static error. From (14) we can get the frequency response by substituting z with $e^{j\omega T}$

$$\dot{G}_i(j\omega)=\frac{\dot{U}_o(j\omega)}{\dot{U}_{ref}(j\omega)}=\frac{k_we^{j\omega T}(g_1e^{j\omega T}+g_2\psi_{12}-g_1\psi_{22})}{l(e^{j\omega T})} \qquad (15)$$

where $\dot{U}_{ref}(j\omega)$ and $\dot{U}_o(j\omega)$ are voltage reference phasor and output voltage phasor respectively. In UPS inverters, the voltage reference u_{ref} is a sine wave with the frequency of 50 Hz, and ω_{ac} is 314 rad/s. The control frequency is 20 kHz in experiment, and the corresponding control period T is 50 μs . Suppose that the actual parameters match the calculating parameters, Fig.6 shows the module and phase of $\dot{G}_i(j\omega_{ac})$ when k_w changes. The steady state error between output voltage and voltage reference increases with the decrease of the value of k_w. When k_w =0.7, the amplitude error is 2%, and the phase error is -0.009° .The system still has good steady state performance.

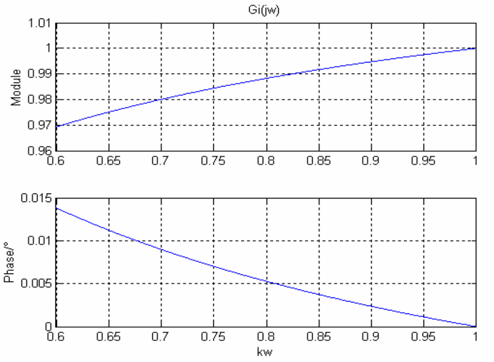


Fig.6 The influence of k_w on steady state performance

The above analysis shows that the modified deadbeat method greatly improves the robust problem which restricts the application of the traditional deadbeat control. This method can be applied into parallel UPS systems to enhance the control performance.

III. PARALLEL OPERATION

Fig. 7 illustrates the structure of a UPS parallel system. Two common lines providing signals s_p* and i_{oa}* are necessary to realize distributed parallel operation. s_p* is a square wave providing frequency and phase information to synchronize voltage references of all the parallel modules. i_{oa}* is the average observed output current of UPS modules.

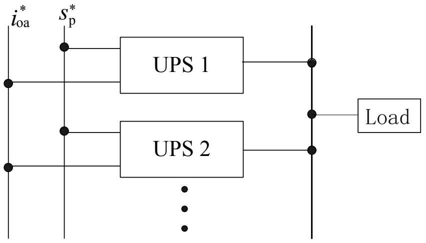


Fig.7 The diagram of a UPS parallel system

A. Synchronization of Output Voltage

The output voltage of each UPS module in a parallel system should have the same amplitude, frequency and phase. Since the voltage control method of each UPS inverter can be simplified as a proportional element, the reference voltage of each UPS modules should be exactly the same.

The amplitude accordance is convenient to realize in digital processor. As the amplitude is stored in the processor as digital quantity, we can simply make the digital quantities of all the UPS in parallel same to each other. The frequency and phase accordance is realized though the common signal s_p*. A common line transmits s_p* to the processor of each UPS, and the processor generates sinusoidal signal according to the phase of s_p*. Figure 8 shows the phase synchronization of the voltage reference u_r* and the signal s_p*.

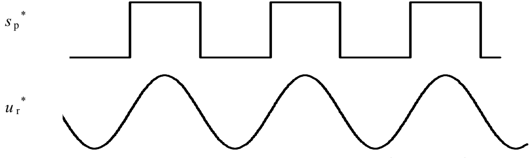


Fig. 8 The phase synchronization of u_r* and s_p*

A phase control unit based on a MCU(micro controller unit) is added to each UPS in order to generate the shared signal s_p*. In this paper, it is realized by DSP. Fig.9 illustrates the phase control unit and its connection to the corresponding common line. s_p* is generated from all the signals s_{pj} by an 'AND' operation,

$$s_p^* = s_{p1} \cap s_{p2} \cap ...... \cap s_{pN} \tag{16}$$

s_{pj} is a phase signal generated by the phase control unit of the UPS j. When AC main is normal (both the RMS value and the frequency are appropriate), signal s_{pj} will trace the phase of AC mains by DPLL(digital phase locked loop). When AC main is abnormal, s_{pj} is generated by the MCU with a crystal of high accuracy. And the MCU adjusts s_{pj} slightly to make it trace s_p*.

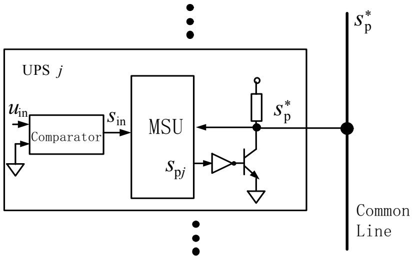


Fig.9 The phase control unit of UPS j

B. Current Sharing Control

Only the synchronization of output voltage cannot guarantee the proper output current distribution among UPS modules. A current sharing control is necessary to adjust the output current of each UPS inverter according to current reference. A common line is used to transmit the instantaneous average current signal i_{oa}* as the reference. Each UPS compares i_{oa}* with its own output current i_{oj}. The voltage reference signal u_r* is adjusted according to the current error signal i_{ocj}. The control scheme is shown in Fig.10.

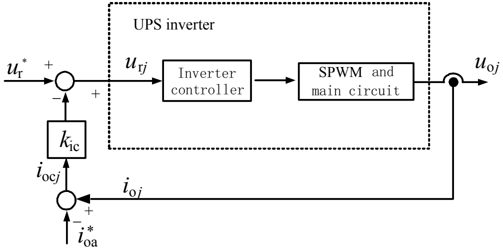


Fig.10 The current sharing control of UPS j

The main circuit of the parallel system is shown in Fig11. L_{lnj} is the inductance of the load line of UPSj, and R_{lnj} is the resistance of the load line. u_{oj} is the output voltage of UPSj, and u_z is the output voltage of the parallel system.

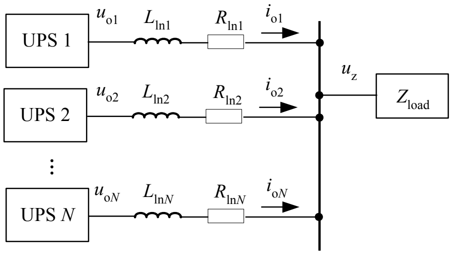


Fig.11 The output side of the UPS parallel system

From Fig.11, it holds

$$\frac{U_{\mathrm{o}1}(s)-U_{\mathrm{z}}(s)}{L_{\mathrm{ln}1}s+R_{\mathrm{ln}1}}+\frac{U_{\mathrm{o}2}(s)-U_{\mathrm{z}}(s)}{L_{\mathrm{ln}2}s+R_{\mathrm{ln}2}}+\ldots+\frac{U_{\mathrm{o}N}(s)-U_{\mathrm{z}}(s)}{L_{\mathrm{ln}N}s+R_{\mathrm{ln}N}}=\frac{U_{\mathrm{z}}(s)}{Z_{\mathrm{load}}(s)} \tag{17}$$

Since it usually holds that $\left|L_{\mathrm{ln}\,j}s+R_{\mathrm{ln}\,j}\right| \ll \left|Z_{\mathrm{load}}(s)\right|$, it can be deduced from (17) that

$$U_{\mathrm{z}}(s)\approx[U_{\mathrm{o}1}(s)+U_{\mathrm{o}2}(s)+\ldots+U_{\mathrm{o}N}(s)]/N \tag{18}$$

Suppose the close-loop transfer function of UPS*j* is G_j(s). To avoid confusion, the output voltage and output current without current sharing control have '0' in the upper right quarter, while the output quantities with current sharing control do not have '0'.

When the current sharing control is not used,

$$U_{\mathrm{o}j}^{0}(s)=G_j(s)U_{\mathrm{r}}^{*}(s) \tag{19}$$

Combining (18) and (19), we can get

$$U_{z}^{0}(s)=\sum_{j=1}^{N}(U_{\mathrm{o}\,j}^{0}(s)/N) \tag{20}$$

Equation (20) shows that without current sharing control, the output voltage of the parallel system is the average of the output voltage of all the UPS inverters in parallel.

When the average current sharing control is used,

$$U_{\mathrm{ref}\,j}(s)=U_{\mathrm{r}}^{*}(s)+k_{\mathrm{ic}}[I_{\mathrm{oa}}^{*}(s)-I_{\mathrm{o}j}(s)] \tag{21}$$

and

$$\begin{aligned}U_{\mathrm{o}j}(s)&=G_j(s)U_{\mathrm{ref}\,j}(s)\\&=U_{\mathrm{o}j}^{0}(s)+G_j(s)k_{\mathrm{ic}}[I_{\mathrm{oa}}^{*}(s)-I_{\mathrm{o}j}(s)]\end{aligned} \tag{22}$$

Combing (18) and (22), we get

$$\begin{aligned}U_{\mathrm{z}}(s)&=\sum_{j=1}^{N}U_{\mathrm{o}j}(s)/N\\&=\sum_{j=1}^{N}[U_{\mathrm{o}j}^{0}(s)+G_j(s)k_{\mathrm{ic}}(I_{\mathrm{oa}}^{*}(s)-I_{\mathrm{o}j}(s))]/N\end{aligned} \tag{23}$$

According to the control law,

$$I_{\mathrm{oa}}^{*}(s)=\sum_{j=1}^{N}I_{\mathrm{o}j}(s)/N \tag{24}$$

The transform functions of the same type UPS inverters are almost the same, namely

$$G_1(s)=G_2(s)=\cdots G_N(s) \tag{25}$$

Combing (23),(24) and (25)

$$U_{\mathrm{z}}(s)=\sum_{j=1}^{N}(U^{0}{}_{\mathrm{o}j}(s)/N)=U_{z}^{0}(s) \tag{26}$$

Equation (26) shows that the current sharing control has no influence on the output voltage of the parallel system, which is still the average output voltage of all the UPS inverters. The current sharing control is independent of the inner voltage control of the UPS inverter.

Since the current sharing control has no influence on it, the output voltage u_{z} can be treated as a disturbance to the current control loop. The control diagram of one inverter with current sharing control is shown as Fig.12. For deadbeat control, $G_j(s)$ can be simplified as a proportional element. According to the classical control theory, the current sharing control element can remain stable no matter what k_{ic} is.

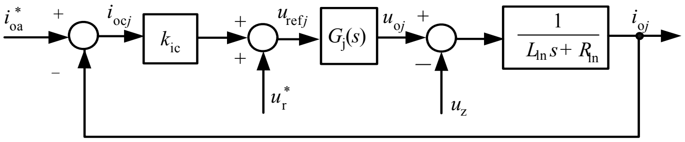


Fig.12 Control diagram of one inverter with current sharing control

According to Fig.11, it holds

$$\dot{U}_{\mathrm{o}\,j}=\dot{I}_{\mathrm{o}\,j}(L_{\mathrm{ln}\,j}\,\mathrm{j}\omega_{\mathrm{ac}}+R_{\mathrm{ln}\,j})+\dot{U}_{\mathrm{z}} \tag{27}$$

where $\omega_{\mathrm{ac}}=314\,\mathrm{rad/s}$.

From (22) we can get

$$(\dot{I}_{\mathrm{oa}}{}^{*}-\dot{I}_{\mathrm{o}\,j})k_{\mathrm{ic}}\dot{G}_{\mathrm{i}}=\dot{U}_{\mathrm{o}\,j}-\dot{U}_{\mathrm{o}\,j}{}^{0} \tag{28}$$

Combining (27) and (28), we get

$$\dot{I}_{\mathrm{o}\,j}(k_{\mathrm{ic}}\dot{G}_{\mathrm{i}}+L_{\mathrm{ln}\,j}\,\mathrm{j}\omega_{\mathrm{ac}}+R_{\mathrm{ln}\,j})=\dot{I}_{\mathrm{oa}}{}^{*}k_{\mathrm{ic}}\dot{G}_{\mathrm{i}}-\dot{U}_{\mathrm{z}}{}^{0}+\dot{U}_{\mathrm{o}\,j}{}^{0} \tag{29}$$

Since the inductance and the resistance of the load line is usually small, it can be

$$|\,L_{\mathrm{ln}\,j}\,\mathrm{j}\omega_{\mathrm{ac}}+R_{\mathrm{ln}\,j}\,|\ll|\,k_{\mathrm{ic}}\dot{G}_{\mathrm{i}}\,| \tag{30}$$

So (29) can be simplified as

$$\dot{I}_{\mathrm{oc}\,j}=\dot{I}_{\mathrm{oa}}^{*}-\dot{I}_{\mathrm{o}\,j}\approx(\dot{U}_{\mathrm{o}\,j}{}^{0}-\dot{U}_{\mathrm{z}})/k_{\mathrm{ic}} \tag{31}$$

From (23) and (31) we get

$$\dot{I}_{\mathrm{oc}\,j}\approx[\dot{U}_{\mathrm{o}\,j}^{0}-\frac{1}{N}\sum_{j=1}^{N}(\dot{U}_{\mathrm{o}\,j}^{0})]/k_{\mathrm{ic}} \tag{32}$$

If U_{or} symbolizes the rated output voltage of single UPS inverter, and Pr symbolizes the relative accuracy of the output voltage (1%~2%), there is

$$I_{\mathrm{oc}\,j}\le 2\,\mathrm{P}_{\mathrm{or}}\,U_{\mathrm{or}}/k_{\mathrm{ic}} \tag{33}$$

It shows that the maximum circular current is only relative to the current sharing control gain k_{ic}, and has no relation with the load of the parallel system. By changing the value of k_{ic}, we can adjust the precision of current sharing control easily.

IV. EXPERIMENTS

A three-cell prototype is built based on DSP TMS320LF2407A to verify the control schemes we proposed here. The parameters are:

Rated output voltage: 100V(rms)/50Hz
Rated capacity: 1KVA/700W
Output filter: *L*=1.3mH, *C*=20μF
Switching frequency: *f*=20 kHz

Fig.13~15 show the output voltage of the system and the output current of each UPS in parallel in different load conditions. They are resistance load, rectifier load, and no load respectively. Table I records the experimental results at heavy load, light load, rectifier load, and no load. The results prove that however the load changes, the system performances satisfactorily. The RMS value of output voltage is in the range of 100V ± 2%, and the THD is below 2%. The current distribution among inverters is proper under all kinds of conditions.

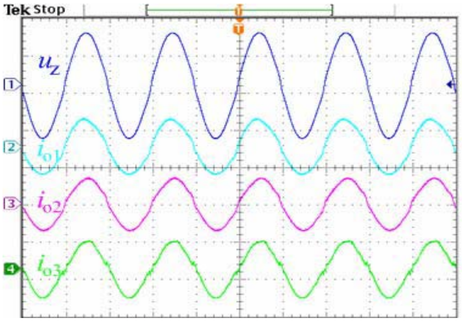


Fig.13 Three modules operating in parallel with resistor load (u_z:100V/div, i_{o1}, i_{o2},and i_{o3}: 5A/div)

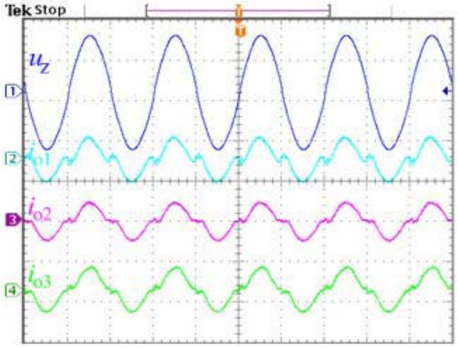


Fig.14 Three modules operating in parallel with rectifier load (u_z:100V/div, i_{o1}, i_{o2},and i_{o3}: 5A/div)

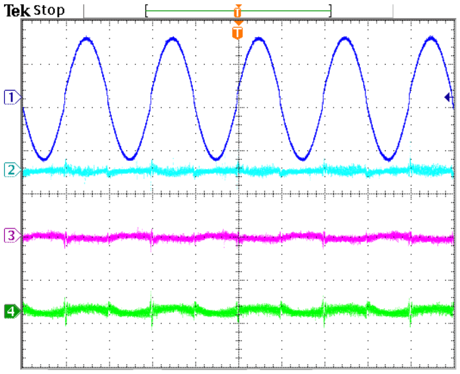


Fig.15 Three modules operating in parallel with no load (u_z:100V/div, i_{o1}, i_{o2},and i_{o3}: 5A/div)

TABLE I

EXPERIMENTAL RESULTS UNDER DIFFERENT CONDITIONS

	U_o (V)	THD of u_o	I_{o1} (A)	I_{o2} (A)	I_{o3} (A)
Heavy load	100.8	1.68%	2.50	2.66	2.60
Light load	101.5	1.67%	1.10	1.32	1.06
Rectifier load	101.5	1.67%	1.62	1.76	1.89
No load	102.0	1.62%	0.37	0.30	0.36

Fig.16 shows the dynamic process when a second UPS is plugged into the parallel. We can see that the current sharing has a fast dynamic response with little disturbance to the output voltage when the load changes.

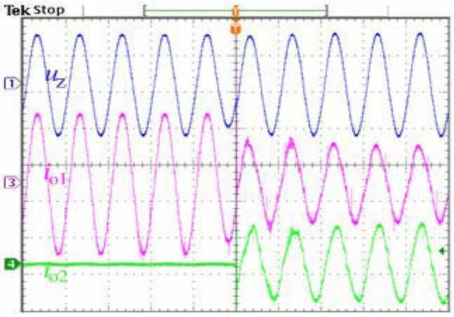


Fig.16 The second UPS plugged into system with rectifier load (u_z:100V/div, i_{o1}, i_{o2}: 5A/div)

V. CONCLUSION

This paper proposes a new way to improve the parallel performance of UPS inverters. Deadbeat control is applied to each UPS inverter in parallel because of its fast dynamic response and good waveform quality. A modified deadbeat control with a proportional element is proposed here to deal with the main drawback of the traditional deadbeat method- the robust problem. A distributed control method is used here to realize parallel operation of UPS modules. The synchronization of output voltages is necessary for parallel operation, and the average current-sharing control ensures the proper load distribution among the modules. The theoretic analysis and experimental results show that the control scheme has several features:

1) The parallel system is simple in structure with only two common lines connecting UPS modules.

2) All UPS modules are exactly the same and real redundancy is achieved.

3) The control scheme is easy to realize in DSP and is insensitive to parametric deviation.

4) Load sharing is precise in dynamic response and steady state.

5) Output voltage has good quality under various kinds of conditions.

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